ON Semiconductor®

TY72011AP2

Advance Information

Single Ended PWM Controller Featuring QR Operation and Soft Frequency Foldback

The TY72011AP2 combines a true Current Mode Control modulator and a demagnetization detector to ensure full Discontinuous Conduction Mode in any load/line conditions and minimum drain voltage switching (Quasi−Resonant operation). Thanks to its inherent Variable Frequency Mode (VFM), the controller decreases its operating frequency at constant peak current whenever the output power demand diminishes. Associated with automatic multiple valley switching, this unique architecture guarantees minimum switching losses and the lowest power drawn from the mains when operating at no−load conditions. The internal High−Voltage current source provides a reliable charging path for the Vcc capacitor and ensures a clean and short start−up sequence without deteriorating the efficiency once off.

Finally, the continuous feedback signal monitoring implemented with an over−current fault protection circuitry (OCP) makes the final design rugged and reliable. An internal Over Voltage Protection (OVP) circuit continuously monitors the Vcc pin and stops the IC whenever its level exceeds 40 V. The internal OVP connection is also externally available to precisely adjust the final protection level to the designer needs.

ORDERING INFORMATION

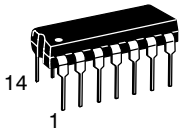
Device	Package	Shipping
TYP2011AP2	PDIP−14	25 Units/Rail
TYP2011AP2G	PDIP−14 (Pb−Free)	25 Units/Rail

Features

- Natural Drain−Source Valley Switching for Lower EMI and Quasi−Resonant Operation
- Current Mode Control
- Smooth Frequency Foldback for Low Standby Power and Minimum Output Ripple at No−Load
- Internal 200 ns Leading Edge Blanking on Current Sense
- Wide UVLO Levels: 9.3 to 15 V Typical
- 250 mA Sink and Source Driver
- Wide Operating Voltages: 8.0 to 36 V with Fixed Over Voltage Protection (OVP) on the V_{CC} or Adjustable through a Dedicated Pin
- Internal Short−Circuit Protection
- Integrated 3.0 mA Typ. Start−Up Source

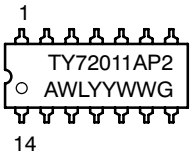
Applications

- Off−Line Charger
- Standby SMPS
- Wall Adapters
- Power Supplies For:
  DVD Players
  Set−Top Boxes, etc.



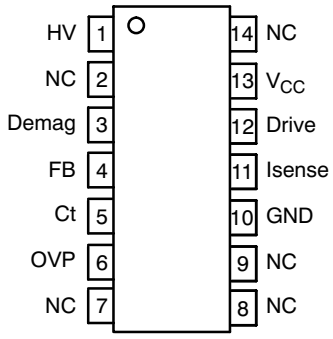
PDIP−14
P SUFFIX
CASE 646

MARKING DIAGRAM



A = Assembly Location
WL = Wafer Lot
YY = Year
WW = Work Week
G = Pb−Free Package

PIN CONNECTIONS



This document contains information on a new product. Specifications and information herein are subject to change without notice.

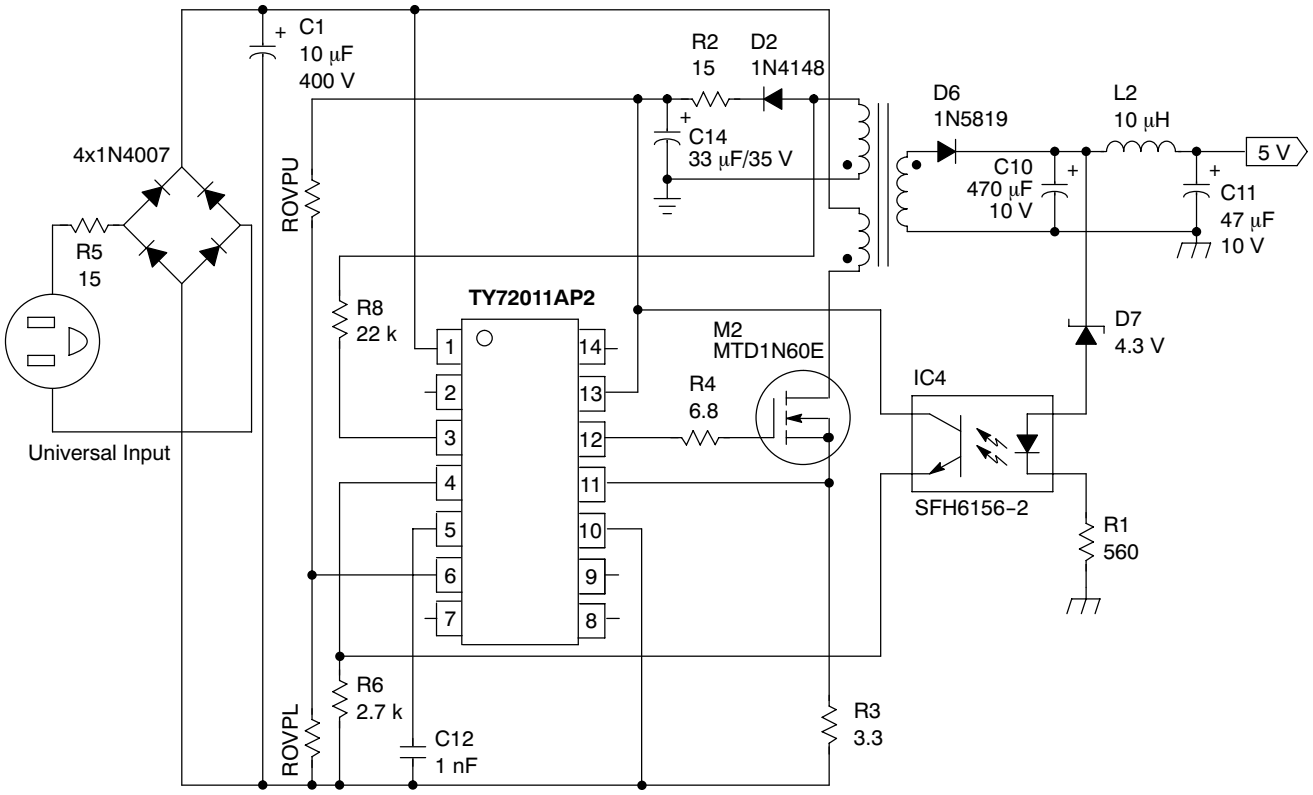


Figure 1. A Typical Off−Line Adapter Application

PIN FUNCTION DESCRIPTION

Pin Number	Pin Name	Function	Description
1	HV	Start−up rail	Connected to the rectified HV rail, this pin provides a charging path to V_{CC} bulk capacitor.
2	NC	−	−
3	Demag	Zero primary−current detection	This pin ensures the re−start of the main switcher when operating in free−run.
4	FB	Feedback signal to control the PWM	This level modulates the peak current level in free−running operation and modulates the frequency in VFM operation.
5	Ct	Timing capacitor	By adding a capacitor from Ct to the ground, the user selects the *minimum* operating frequency.
6	OVP	Overvoltage pin	By applying a level of 2.8 V typical on this pin, the IC is permanently latched−off until V_{CC} falls below $UVLO_L$.
7	NC	−	−
8	NC	−	−
9	NC	−	−
10	Gnd	The IC's ground	−
11	Isense	The primary−current sensing pin	This pin senses the primary current via an external shunt resistor.
12	Drv	This pin drives the external switcher	The IC is able to deliver or absorb 250 mA peak currents while delivering a clamped driving signal.
13	V_{CC}	Powers the IC	A positive voltage up to 40 V *typical* can be applied upon this pin before the IC stops.
14	NC	−	−

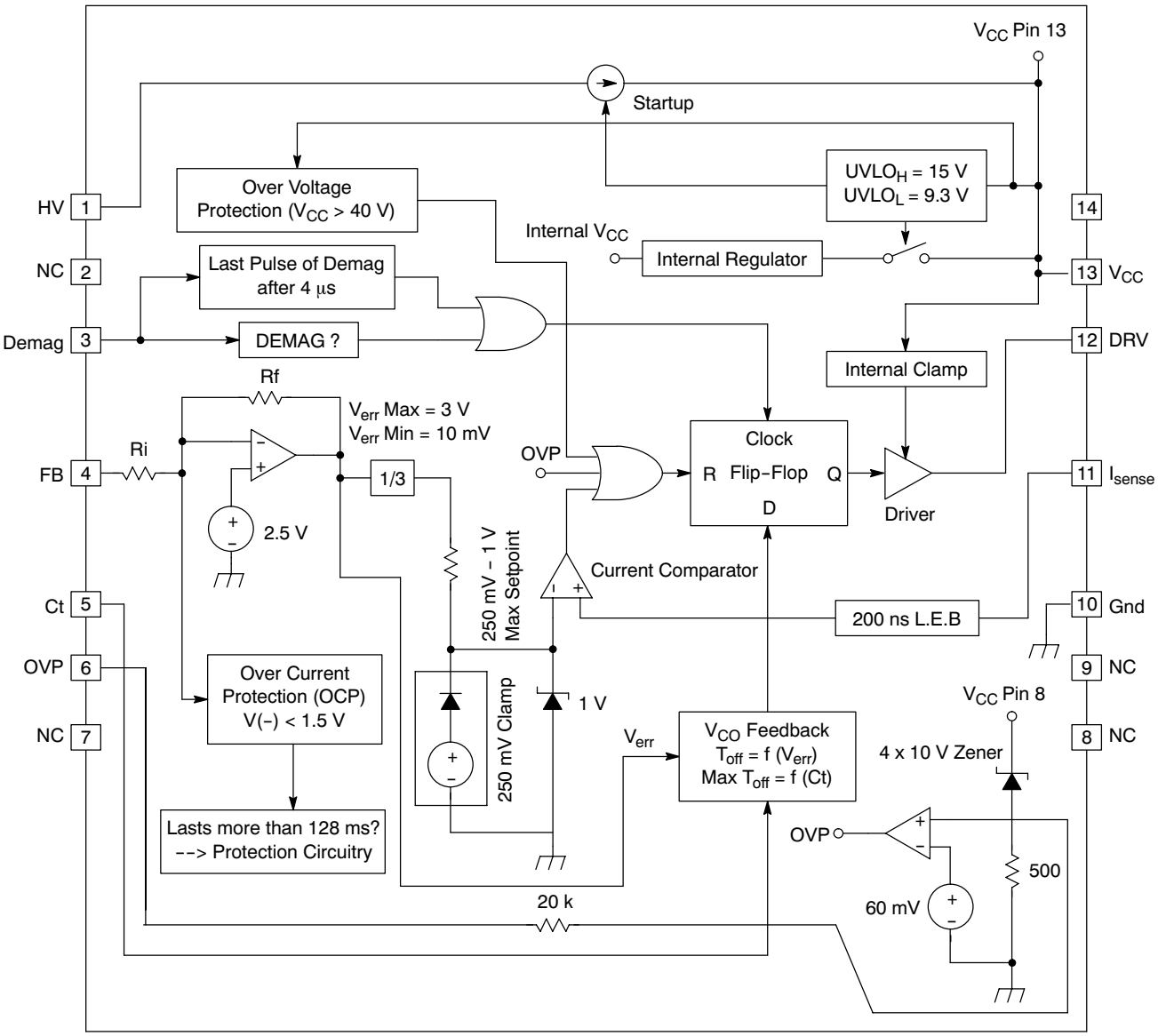


Figure 2. Simplified Block Diagram

MAXIMUM RATINGS

Rating	Pin #	Symbol	Value		Unit
			Min	Max	
Power Supply Voltage	8	V_{in}	–	45	V
Thermal Resistance Junction–to–Air	–	$R_{\theta JA}$	–	100	°C/W
Operating Ambient Temperature Maximum Junction Temperature	–	T_A T_{Jmax}	–	–25 to +85 150	°C °C
Storage Temperature Range	–	T_{stg}	–	–60 to +150	°C
ESD Capability, HBM Model	All Pins	–	–	2.0	kV
ESD Capability, Machine Model	All Pins	–	–	200	V
Demagnetization Pin Current	3	–	–	±5.0	mA

ELECTRICAL CHARACTERISTICS (For typical values T_A = 25°C, for min/max values T_A = –25°C to +85°C, Max T_J = 150°C, V_{CC} = 12 V unless otherwise noted.)

Characteristics	Pin #	Symbol	Min	Typ	Max	Unit
Demagnetization Block						
Input Threshold Voltage (V_{pin2} increasing)	3	Vth	50	65	85	mV
Hysteresis (V_{pin2} decreasing)	3	V_H	–	30	–	mV
Input Clamp Voltage High State (I_{pin2} = 3.0 mA) Low State (I_{pin2} = –3.0 mA)	3	 VC_H VC_L	 8.0 –0.9	 10 –0.7	 12 –0.5	V
Demag Propagation Delay	–	–	100	300	350	ns
No Demag Signal Activation	–	–	–	4.0	8.0	μs
Internal Input Capacitance at 1.0 V	3	C_{pin3}	–	10	–	pF
Demag Propagation Delay with 22 kΩ External Resistor	3	–	100	370	480	ns
Feedback Path (For typical values T_A = 25°C, for min/max values T_A = –25°C to +85°C, Max T_J = 125°C unless otherwise noted.)						
Input Impedance at V_{FB} = 3.0 V	4	Zin	–	50	–	kΩ
Internal Error Amplifier Closed Loop Gain	4	AV_{CL}	–	–3.0	–	–
Internal Built–In Offset Voltage for Error Detection	–	Vref	2.2	2.5	2.8	V
Error Amplifier Level of VCO Take Over	–	–	–	1.0	–	V
Internal Divider from Internal Error Amp, Pin to Current Setpoint	–	–	–	3.0	–	–
Fault Detection Circuitry						
Internal Over Current Level	–	WL_L	–	1.5	–	V
Fault Time Duration to Latch Activation @ Ct = 1.0 ηF	–	–	–	128	–	ms
Over Current Latch–Off Phase @ Ct = 1.0 ηF	–	–	–	1.02	–	s
Hysteresis when V_{FB} goes back into Regulation	–	–	–	100	–	mV
V_{CC} (Pin 13) Over Voltage Protection	13	OVP1	36	40	43	V
Over Voltage Protection	6	OVP2	2.5	2.8	3.1	V
Current Comparator						
Input Bias Current @ 1.0 V	11	I_{IB}	–	0.02	–	μA
Maximum Current Setpoint	11	Vcl	0.9	1.0	1.1	V
Minimum Current Setpoint	11	V_{min}	225	250	285	mV

ELECTRICAL CHARACTERISTICS (continued) (For typical values T_A = 25°C, for min/max values T_A = −25°C to +85°C, Max T_J = 150°C, V_{CC} = 12 V unless otherwise noted.)

Characteristics	Pin #	Symbol	Min	Typ	Max	Unit
Current Comparator (continued)						
Propagation Delay from Current Detection to Gate OFF State	11	Tdel	–	200	250	ns
Leading Edge Blanking (LEB)	11	Tleb	–	200	–	ns
Variable Frequency Modulator						
Minimum Frequency Operation @ Ct = 1.0 ηF and V_{CC} = 35 V	5	Fmin	–	0	–	kHz
Maximum Frequency Operation @ Ct = 1.0 ηF and V_{CC} = 35 V	5	Fmax	90	110	125	kHz
Minimum Ct Charging Current (Note 1)	5	I_{Ct}min	–	0	–	μA
Maximum Ct Charging Current (Note 1)	5	I_{Ct}max	280	350	420	μA
Discharge Time @ Ct = 1.0 ηF	5	–	–	500	–	ns
Drive Output						
Output Voltage Rise Time @ C_L = 1.0 ηF (ΔV = 10 V)	12	tr	–	60	100	ns
Output Voltage Fall Time @ C_L = 1.0 ηF (ΔV = 10 V)	12	tf	–	40	100	ns
Clamped Output Voltage @ V_{CC} = 35 V (Note 2)	12	V_{DRV}	11	13	16	V
Voltage Drop on the Stage @ V_{CC} = 10 V (Note 2)	12	V_{DRV}	–	–	0.5	V
Undervoltage Lockout						
Startup Threshold (V_{CC} Increasing)	13	$UVLO_H$	13.5	15	16.5	V
Minimum Operating Voltage (V_{CC} Decreasing)	13	$UVLO_L$	8.3	9.3	10.0	V
Internal Startup Current Source						
Maximum Voltage, Pin 1 Grounded	1	–	–	450	–	V
Maximum Voltage, Pin 1 Decoupled (470 μF)	1	–	–	500	–	V
Startup Current Flowing through Pin 1	1	–	2.5	3.0	4.5	mA
Leakage Current in Offstate @ Vpin 1 = 500 V	1	–	–	32	70	μA
Device Current Consumption						
V_{CC} less than $UVLO_H$	13	–	–	1.5	1.8	mA
V_{CC} = 35 V and Fsw = 2.0 kHz, C_L = 1.0 ηF	13	–	–	1.2	3.0	mA
V_{CC} = 35 V and Fsw = 125 kHz, C_L = 1.0 ηF	13	–	–	3.0	4.0	mA
Startup Current to V_{CC} Capacitor	13	–	1.5	–	–	mA

1. Typical capacitor swing is between 0.5 V and 3.5 V.
2. Guaranteed by design, T_J = 25°C.

THEORY OF OPERATION

Introduction

By implementing a unique smooth frequency reduction technique, the TY72011 represents a major leap toward low−power Switch−Mode Power Supply (SMPS) integrated management. The circuit combines free−running operation with minimum drain−source switching (so−called valley switching), which naturally reduces the peak current stress as well as the ElectroMagnetic Interferences (EMI). At nominal output power, the circuit implements a traditional current−mode SMPS whose peak current setpoint is given by the feedback signal. However, rather than keeping the switching frequency constant, each cycle is initiated by the end of the primary demagnetization. The system therefore operates at the boundary between Discontinuous Conduction Mode (DCM) and Continuous Conduction Mode (CCM). Figure 3 details this terminology:

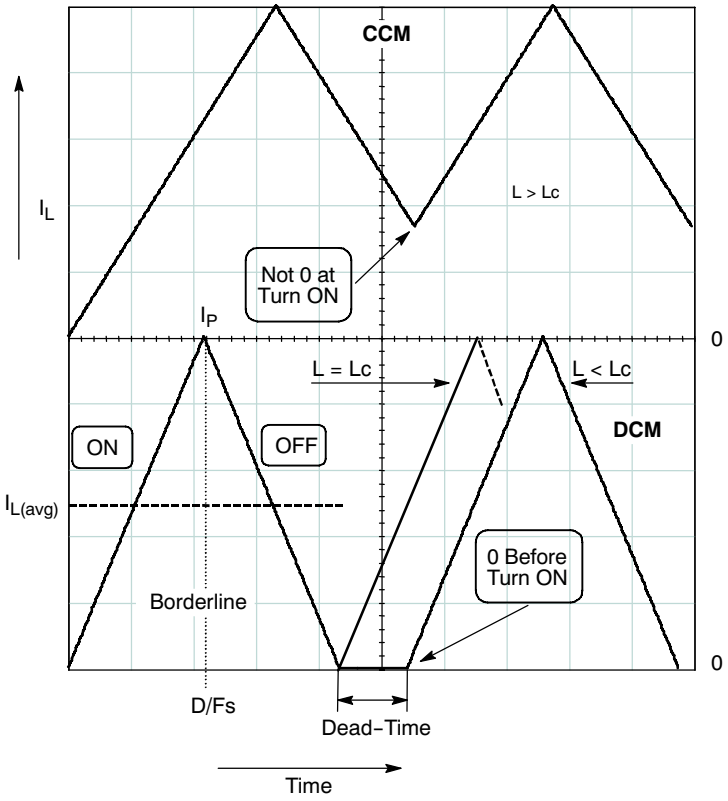


Figure 3.

When the output power demands decreases, the natural switching frequency raises. As a natural result, switching losses also increase and degrade the SMPS efficiency. To overcome this problem, the maximum switching frequency of the TY72011 is clamped to typically 125 kHz. When the free running mode (also called Borderline Control Mode, BCM) reaches this clamp value, an internal Voltage−Controlled Oscillator (VCO) takes over and starts to decrease the switching frequency: we are in Variable Frequency Mode (VFM). Please note that during this transition phase, the peak current is not fixed but is still decreasing because the output power demand does. At a given state, the peak current reaches a minimum height (typically 250 mV/Rsense), and cannot go further down: the switching frequency continues its decrease down to a possible minimum of 0 Hz (the IC simply stops switching). During normal free−running operation and VFM, the controller always ensures single or multiple drain−source valley switching. We will see later on how this is internally implemented.

The FLYBACK operation is mainly defined through a simple formula:

$$Pout = \frac{1}{2} \cdot Lp \cdot Ip^2 \cdot Fsw \qquad \text{(eq. 1)}$$

With:

Lp the primary transformer inductance (also called the magnetizing inductance)

Ip the peak current at which the MOSFET is turned off

Fsw the nominal switching frequency

To adjust the transmitted power, the PWM controller can play on the switching frequency or the peak current setpoint. To refine the control, the TY72011 offers the ability to play on both parameters either altogether or on an individual basis.

In order to clarify the device behavior, we can distinguish the following *simplified* operating phases:

1.
The load is at its nominal value. The SMPS operates in borderline conduction mode and the switching frequency is imposed by the external elements (Vin, Lp, Ip, Vout). The MOSFET is turned on at the minimum drain−source level.
2.
The load starts to decrease and the free−running frequency hits the internal clamp.
3.
The frequency can no longer naturally increase because of the clamp. The frequency is now controlled by the internal VCO but remains constant. The peak current finds no other option that diminishing to satisfy equation (1).
4.
The peak current has reached the internal minimum ceiling level and is now frozen for the remaining cycles.
5.
To further reduce the transmitted power (V_{FB} goes up), the VCO decreases the switching frequency. In case of output overshoot, the VCO could decrease the frequency down to zero. When the overshoot has gone, V_{FB} diminishes again and the IC smoothly resumes its operation.

Advantages of the Method

By implementing the aforementioned control scheme, the TY72011 brings the following advantages:

- Discontinuous only operation: in DCM, the FLYBACK is a first order system (at low frequencies) and thus naturally eases the feedback loop compensation.
- A low−cost secondary rectifier can be used thanks to smooth turn−off conditions.
- Valley switching ensures minimum switching losses brought by Coss and all the parasitic capacitances.
- By folding back the switching frequency, you turn the system into Pulse Duration Modulation. This method prevents from generating *uncontrolled* output ripple as with hysteretic controllers.
- By letting you control the peak current value at which the frequency goes down, you ensure that this level is low enough to avoid transformer acoustic noise generation even at audible frequencies.

Detailed Description

The following sections describe the internal behavior of the TY72011.

Free−Running Operation

As previously said, the operating frequency at nominal load is dictated by the external elements. We can split the different switching sections in two separated instants. In the following text we use the internal error voltage, Verr. This level is elaborated as Figure 7 portrays. Verr is linked to VFB (pin 4) by the following formula: $Verr = 10 - 3 \cdot V_{FB}$

ON time: the ON time is given by the time it takes to reach the peak current setpoint imposed by the level on FB pin (pin 4). Since this level is internally divided by three, the peak setpoint is simply:

$$Ipk = \frac{1}{3 \cdot Rsense} \cdot Verr \qquad \text{(eq. 2)}$$

The rising slope of the peak current is also dependent on the inductance value and the rectified DC input voltage by:

$$\frac{dIL}{dt} = \frac{Vin_{DC}}{Lp} \qquad \text{(eq. 3)}$$

By combining both equations, we obtain the ON time definition:

$$ton = \frac{Lp}{Vin_{DC}} \cdot Ip = \frac{Lp \cdot V_{ERR}}{Vin_{DC} \cdot 3 \cdot Rsense} \qquad \text{(eq. 4)}$$

OFF time: the time taken by the demagnetization of the transformer depends on the reset voltage applied at the switch opening. During the conduction time of the secondary diode, the primary side of the transformer undergoes a reflected voltage of: [Np/Ns . (Vf + Vout)]. This voltage applied on the primary inductance dictates the time needed to decrease from Ip down to zero:

$$toff = \frac{Lp}{\left[\frac{Np}{Ns} \cdot (Vout + Vf)\right]}$$

$$\cdot Ip = \frac{Lp \cdot Verr}{\left[\frac{Np}{Ns} \cdot (Vout + Vf)\right] \cdot 3 \cdot Rsense} \qquad \text{(eq. 5)}$$

By adding ton + toff, we obtain the natural switching frequency of the SMPS operating in Borderline Conduction Mode (BCM):

$$ton + toff = \frac{Verr \cdot Lp}{3 \cdot Rsense} \cdot \left[\frac{1}{Vin_{DC}} + \frac{1}{\left[\frac{Np}{Ns} \cdot (Vout + Vf)\right]}\right] \qquad \text{(eq. 6)}$$

If we now enter this formula into a spreadsheet, we can easily plot the switching frequency versus the output power demand:

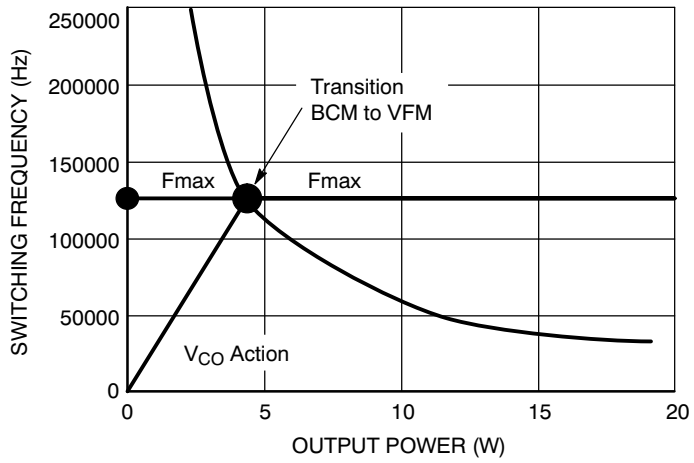


Figure 4. Free Running Frequency vs. Output Power

The typical above diagram shows how the frequency moves with the output power demand. The components used for the simulation were: Vin = 300 V, Lp = 6.5 mH, Vout = 10 V, Np/Ns = 12.

The red line indicates where the maximum frequency is clamped. At this time, the VCO takes over and decreases the switching frequency to the minimum value.

VCO Operation

The VCO is controlled from the Verr voltage. For Verr levels *above* 1.0 V, the VCO frequency remains unchanged at 125 kHz. As soon as Verr starts to decrease below 1.0 V, the VCO frequency decreases with a typical *small−signal* slope of −175 kHz/mV @ Verr = 500 mV down to zero (typically at FB ≈ 3.3 V). The demagnetization synchronization is however kept when the Toff expands. The maximum switching frequency can be altered by adjusting the Ct capacitor on pin 5. The 125 kHz maximum operation ensures that the fundamental component stays external from the international EMI CISPR−22 specification beginning.

The following drawing explains the philosophy behind the idea:

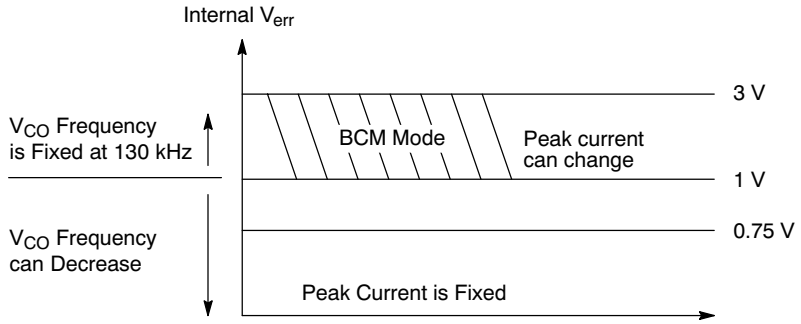


Figure 5.

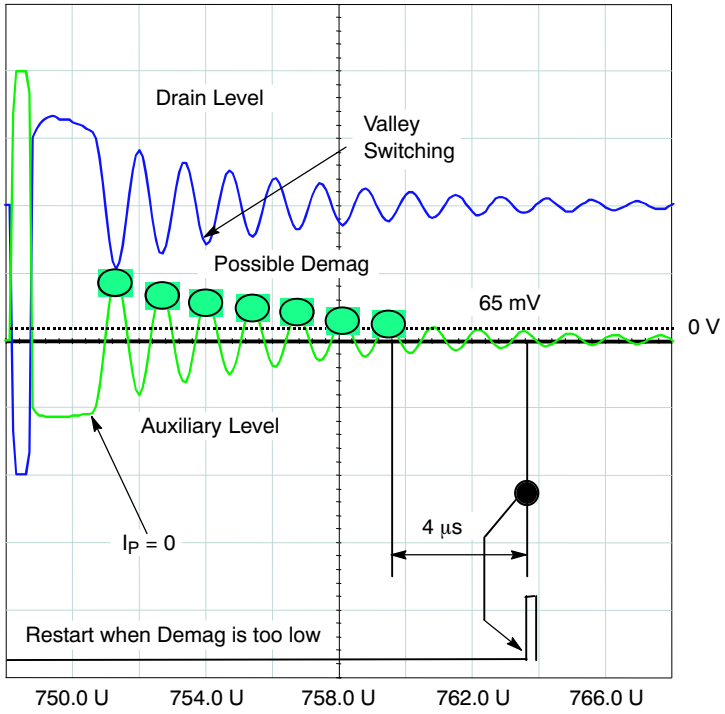


Figure 6.

Zero Crossing Detector

To detect the zero primary current, we make use of an auxiliary winding. By coupling this winding to the primary, we have a voltage image of the flux activity in the core. Figure 6 details the shape of the signal in BCM.

The auxiliary winding for demagnetization needs to be wired in FORWARD mode only. As Figure 6 depicts, when the MOSFET closes, the auxiliary winding delivers (Naux/Np . Vin). At the switch opening, we couple the auxiliary winding to the main output power winding and thus deliver: (−Naux/Ns . Vout). When DCM occurs, the ringing also takes place on the auxiliary winding. As soon as the level crosses−up the internal reference level (65 mV), a signal is internally sent to re−start the MOSFET. Three different conditions can occur:

1.
In BCM, every time the 65 mV line is crossed, the switch is immediately turned−on. By accounting for the internal Demag pin capacitance (10−15 pF typical), you can introduce a fixed delay, which, combined to the propagation delay, allows to precisely re−start in the drain−source valley (minimum voltage to reduce capacitive losses).

2.
When the IC enters VFM, the VCO delivers a pulse which is internally latched. As soon as the demagnetization pulse appears, the logic re−starts the MOSFET.

3.
As can be seen from Figure 6, the parasitic oscillations on the drain are subject to a natural damping, mainly imputed to ohmic losses. At a given point, the demag activity on the auxiliary winding becomes too low to be detected. To avoid any re−start problem, the TY72011 features an internal 4.0 µs timeout delay. This timeout runs after each demag pulse. If within 4.0 µs further to a demag pulse no activity is detected, an internal signal is combined with the VCO to actually re−start the MOSFET (synchronized with Ct).

Error Amplifier and Fault Detection

The TY72011 features an internal error amplifier solely used to detect an overcurrent problem. The application assumes that all the error gain associated with the precise reference level is located on the secondary side of the SMPS. Various solutions can be purposely implemented such as the TL431 or a dedicated circuit like the MC33341. In the TY72011, the internal OPAMP is used to create a virtual ground permanently biased at 2.5 V (Figure 7), an internal reference level. By monitoring this virtual ground further called V(−), we have the possibility to confirm the good behavior of the loop. If by any mean the loop is broken (shorted optocoupler, open LED etc.) or the regulation cannot be reached (true output short−circuit), the OPAMP network is adjusted in order to no longer be able to ensure the 2.5 V virtual point V(−). If V(−) passes down the 1.5 V level (e.g. output shorted) for a time longer than 128 ms, then the pulses are stopped for 8 x 128 ms. The IC enters a kind of burst mode with bunch of pulses lasting 128 ms and repeating every 8 x 128 ms. If the loop is restored within the 8 x 128 ms period, then the pulses are back again on the output drive (synchronized with $UVLO_H$).

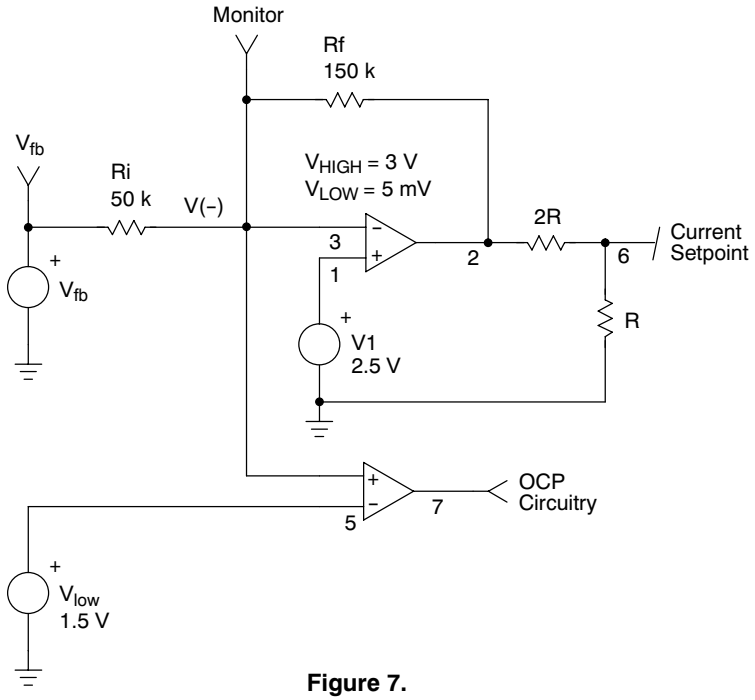


Figure 7.

To illustrate how the system reacts to a variable FB level, we have entered the above circuit into a SPICE simulator and observed the output waveforms. When FB is within regulation, the error flag is low. However, as soon as FB leaves its normal operating area, the OPAMP can no longer keep the V(−) point and either goes to the positive top or down to zero: the error flag goes high.

Because of the large amount of delay necessary for this 128 ms operation, the capacitor used for the timing is Ct, connected from ground to pin 5. In normal VFM operation, this timing capacitor serves as the VCO capacitor and the error management circuit is transparent. As soon as an error is detected (error flag goes high), an internal switch routes Ct to the 128 ms generator. As a first effect, the switching frequency is no longer controlled by the VCO (if the error appears during VFM) and the system is relaxed to natural BCM. The capacitor now ramps up and down to be further divided and finally create the 128 ms delay.

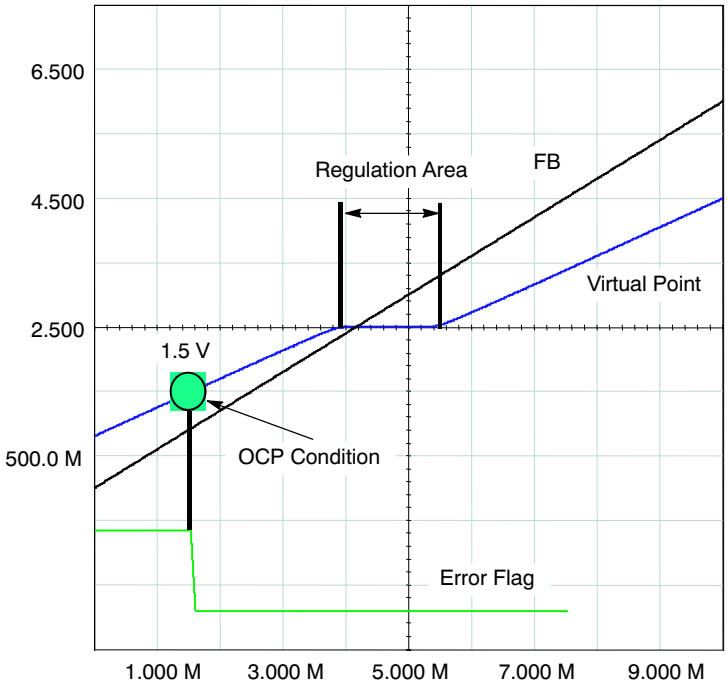


Figure 8.

As soon as the system recovers from the error, e.g. FB is back within its regulation area, the IC operation comes back to normal.

To avoid any system thermal runaway, another internal 8 x 128 ms delay is combined with the previous 128 ms. It works as follow: the 128 ms delay is provided to account for any normal transients that engender a temporary loss of feedback (FB goes toward ground). However, when the 128 ms period is actually over (the feedback is definitively lost) the IC stops the output driving pulses for a typical period of 8 x 128 ms. During this mode, the rest of the functions are still activated. For instance, in lack of pulses, the self−supplied being no longer provided, the start−up source turns on and off (when reaching the corresponding $UVLO_L$ and $UVLO_H$ levels), creating an hiccup waveform on the Vcc line. As soon as the feedback condition is restored, the 8 x 128 ms is interrupted and, in synchronism with the Vcc line, the IC is back to normal. The following diagrams show how this mechanism takes place when FB is down to zero (optocoupler opened) or up to Vcc (optocoupler shorted). If we assume that the error is permanently present, then a burst mode takes place with a 128/8 x 128 = 12.5% duty−cycle. The real transmitted power is thus:

$$Pout_{BURST} = \frac{1}{2} \cdot Lp \cdot Ip^2 \cdot Fsw \cdot Duty_{BURST}$$

Over Voltage Conditions (OVP) are detected by monitoring the Vcc level. As Figure 9 describes, three 10 V zener plus one 5.0 V zener are connected in series together with a 18 kΩ to ground. As soon as Vcc exceeds 40 V *typical*, a current starts to flow in the 18 k resistor. When the voltage developed across this element exceeds 2.5 V, an error is triggered and immediately latches the IC off. In lack of switching pulses, the Vcc capacitor is no longer refreshed by the auxiliary supply and slowly discharges toward ground. When the Vcc level crosses $UVLO_L$, a new startup sequence occurs. If the OVP has gone, normal IC operation takes place. For different OVP levels, the comparator input is accessible through pin 6.

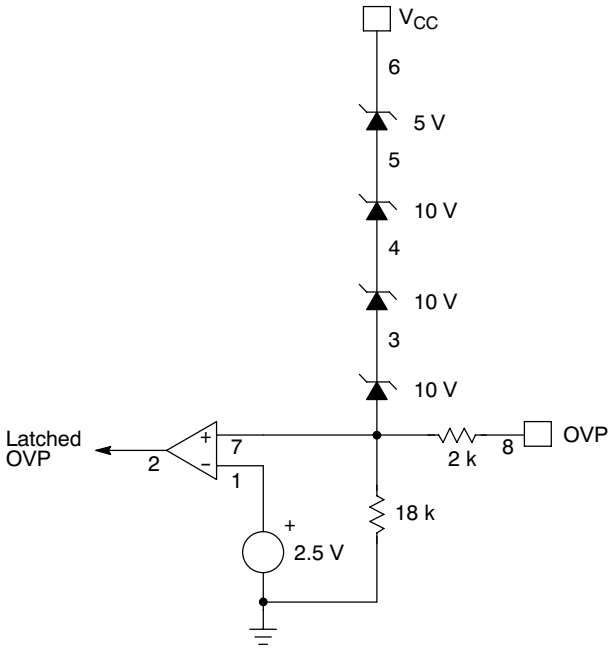


Figure 9.

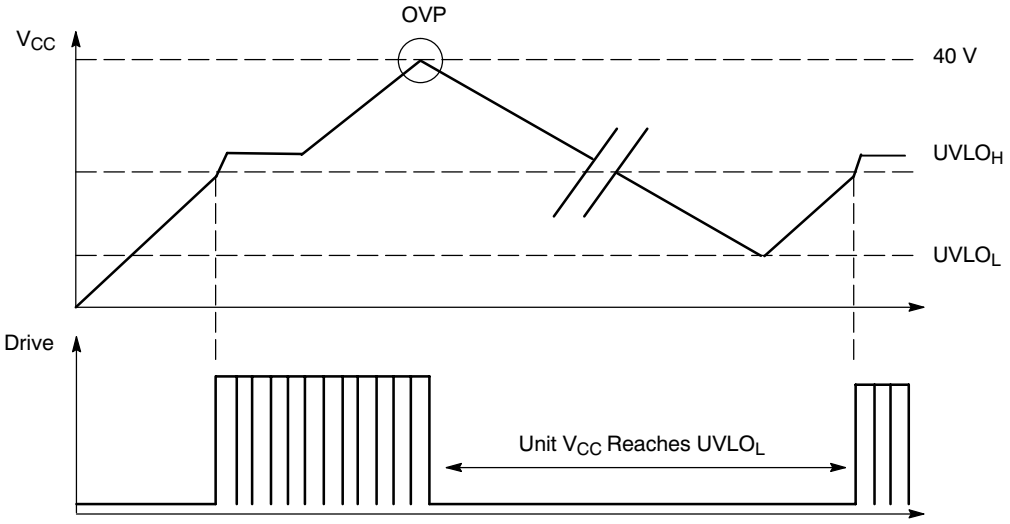


Figure 10. Over Voltage Protection Diagram

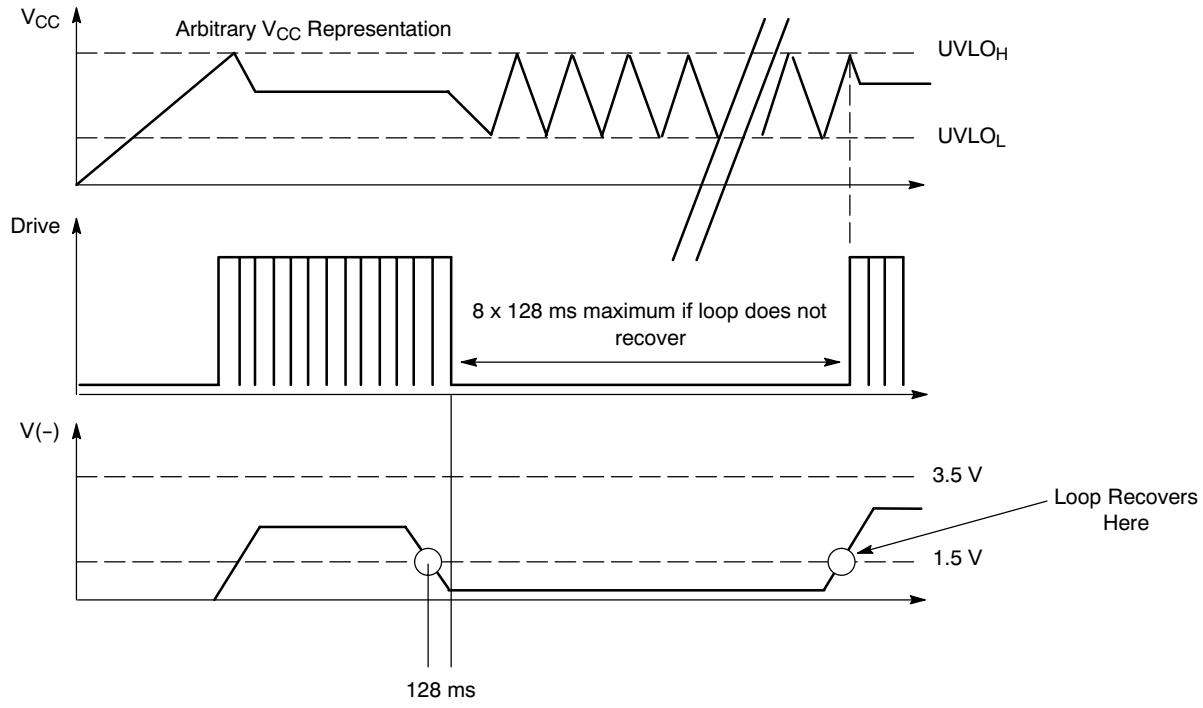
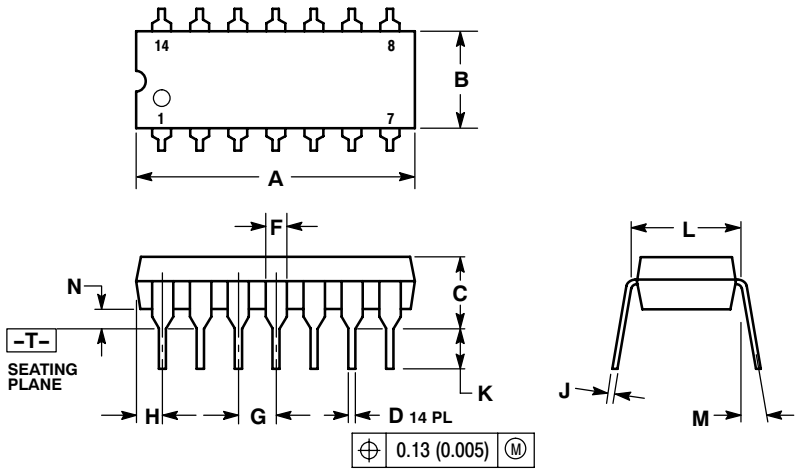


Figure 11. V(−) Level Passes Under 1.5 V

TY72011AP2

PACKAGE DIMENSIONS

PDIP−14
CASE 646−06
ISSUE P



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
4. DIMENSION B DOES NOT INCLUDE MOLD FLASH.
5. ROUNDED CORNERS OPTIONAL.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.715	0.770	18.16	19.56
B	0.240	0.260	6.10	6.60
C	0.145	0.185	3.69	4.69
D	0.015	0.021	0.38	0.53
F	0.040	0.070	1.02	1.78
G	0.100 BSC		2.54 BSC	
H	0.052	0.095	1.32	2.41
J	0.008	0.015	0.20	0.38
K	0.115	0.135	2.92	3.43
L	0.290	0.310	7.37	7.87
M	---	10 °	---	10 °
N	0.015	0.039	0.38	1.01

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